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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,604	08/07/2001	Friedrich Hapke	DE 000118	1419

24737 7590 05/12/2004

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/12/2004

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/923,604	Applicant(s) HAPKE, FRIEDRICH	
	Examiner John P Trimmings	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to applicant's amendment and request for reconsideration dated 3/15/2004.

Response to Amendment

The examiner acknowledges applicant's amendments to Claims 1-3.

The examiner acknowledges applicant's changes to the Abstract.

The examiner acknowledges applicant's changes to the specification.

The examiner acknowledges applicant's request for approval of a drawing change to FIG.2, and approves the same.

Response Re: Claim Rejections - 35 USC § 103

Applicant's arguments, see amendment, filed 3/15/2004, with respect to Claims 1-3 have been fully considered and are persuasive. The rejection of Claims 1 and 3 has been withdrawn. Subsequently, the examiner's rejection to dependent Claim 2 is also withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasuya, U.S. Patent No. 4366393, in view of Patel et al., U.S. Patent No. 5377197, and further in view of Hamzaoglu et al., "Compact Two-Pattern Test Set Generation for Combinational and Full Scan Circuits",. Kasuya substantially teaches a test circuit and a method (column 1 lines 65-68 and column 2 lines 1-2), which arrangement performs a test of the behavior of the combinational logic system (Kasuya column 1 lines 5-10). The test circuit, in a test mode (Kasuya FIG.1 A 103), applies a first test sample (Kasuya FIG.1 106), in a first test clock cycle (Kasuya FIG.1 C&A) to the input of the combinational logic system of the integrated circuit (Kasuya FIG.1 1), and receives the output signal in a buffer memory (Kasuya FIG.1 2), and which feeds back this output signal (Kasuya FIG.1 Y) as a second test sample in a second test clock cycle (Kasuya FIG.1 Y") to the input of the combinational logic system (Kasuya FIG.1 Y') and again receives the output signal of the combinational logic system in the buffer memory (Kasuya FIG.1 Y), the buffer circuit being constituted as a shift register (Kasuya column 2 lines 3-9). And wherein the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory (Kasuya FIG.1 2, 110 and column 3 lines 18-28). Kasuya however fails to teach that, at the end of the second test clock cycle, the arrangement compares the buffer with the results of a second software model. But the method of Patel et al. (see Patel et al. Abstract), in an analogous art,

using the same circuit as Kasuya (Patel et al. FIG.2), does teach this feature by using an Iterative Logic Array representation (FIG.3) of the circuit (FIG.2), and applying the ILA methods in column 5 lines 4-25. It would have been obvious to one with ordinary skill to modify the arrangement of Kasuya based on the method of Patel et al. because the circuits are identical, and are based on the ILA approach. And Patel et al. describes the advantage as being a better way to generate the most effective test vectors in a test circuit. But neither of the references of Kasuya and Patel et al. indicates the operation of this ILA circuit occurs within two clock pulses. However, in an analogous art, Hamzaoglu et al. teaches an arrangement for testing an integrated circuit (page 949 column 2 paragraph 3 lines 1-5) using a "two-pattern" test technique, comprising a combinational logic system (page 950 column 1 paragraph 1 last 3 lines) and a test circuit, which arrangement performs a test of the behavior of the combinational logic system in the same manner as Patel et al. (Hamzaoglu et al. FIG.4) in comparison with test software which emulates the nominal behavior of the integrated circuit (page 944 column 2 2nd paragraph), the arrangement comprising: two identical software models of the combinational logic system to be tested (page 950 column 1 1st paragraph), in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models, and at the end of the second test clock cycle, the arrangement compares the output with the results of a second software model. (page 950 column 1 paragraph 2 and column 2). It would have again been obvious to perform the test steps as described by Hamzaoglu et al. on the circuit of Kasuya and Patel et al., because the circuits under consideration were all the

exact same circuits. And Hamzaoglu et al., on page 944 column 2 paragraph 2, boasts of a way to generate two-pattern test vectors in order to test circuit response/rise time, using a smaller and more effective test vector arrangement. And one with ordinary skill in the art at the time of the invention, motivated as suggested by both Patel et al. and Hamzaoglu et al., would combine the references, and so the Claims 1-3 are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Examiner
Art Unit 2133

jpt